Proceedings of the 8th Conference (1976 International) on Solid State Devices, Tokyo, 1976;
Japanese Journal of Applied Physics, Volume 16 (1977) Supplement 16-1, pp. 151–154

Static Induction Logic-A Simple Structure with Very Low Switching Energy and Very High Packing Density

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The new logic structure using static induction transistor is presented. This logic structure has very low delay-power product, and order below 0.01 pJ is possible. High current gain of presented transistor makes *n*-diffusion isolation layer between gates unnecessary and allows high packing dencity, higher than 1000 gate/mm^2. Standard technological process requires the 4-masking steps only, however 3-mask technology is also presented.

§1. Introduction

The trend in integrated logic circuit design drives toward the reduction of both the delay time and the supply power. The I^{2}L structure[1,2] offers the lowest switching energy at present. Further reduction of this energy of about two times can be achieved in the VIL structure[3] in which the supply power efficiency has been increased due to the increased injector current gain. However, the VIL structure requires eight masking steps. The new type of transistor with simple structure introduced here allows further reduction in the power-delay product. Also the number of fabrication processes is far reduced.

§2. Low Delay-Power Product

The delay-power product is expressed by the term:

$$\tau \times P = \frac{\alpha_v}{\alpha_i} V_b^2 C_t \qquad (1)$$

where

$\alpha_v = V_{sw}/V_b$—ratio of the voltage-swing V_{sw} between two logical levels to the supply voltage V_b

$\alpha_i = I_i/I_b$—ratio of the injector current I_i to the supply current I_b

V_b—supply voltage

C_t—total gate capacitance, $C_t = C_{eb} + 2C_{bc}$ in I^{2}L case.

However the low value of α_v makes low switching energy (see eq. (1)), but it also leads to the lowering of logic noise immunity. Therefore in order to have reasonable noise margin, the value of α_v should be close to unity. Also α_i which correspond to injector current gain should be close to unity. The equation (1) can be then rewritten in the form as follows,

$$\tau \times P \approx V_b^2 C_t \qquad (2)$$

If the circuit dimension remain constant due to the photolithography process limitation, the small time delay product can be obtained by lowering the impurity concentration which leads to lowering the capacitance C_t. The other method of the significant reduction of the $\tau \times P$ product is to decrease of the supply voltage V_b. In the case of I^{2}L the lowest value of this voltage is limited by the built-in field on emitter junction of *npn* transistor. Some reduction in this voltage is also possible in I^{2}L by decreasing the impurity concentration in base of *npn* transistor. This however leads to other undesired effects such as the increasing of base series resistances and the decreasing of injection efficiency of *pnp* injectors.

§3. The New Type of Transistor

Let us considere two types of transistor structures presented in Fig. 1(a) and (b). Transistor in Fig. 1(a) can be considered as usual bipolar transistor in which base region has been obtained by lateral *p*-type diffusion. Therefore in the center of the base region the impurity concentration is lowest. Most of injected carriers from emitter go through this lowly doped region in the base center, since also the potential barrier hight is lowest in this region. This potential barrier hight V_h for transistor structure presented in Fig. 1(a) is equal:

$$V_{h1} = \frac{kT}{q} \ln\left(\frac{N_e N_b}{n_i^2} - V_{be}\right) \qquad (3)$$

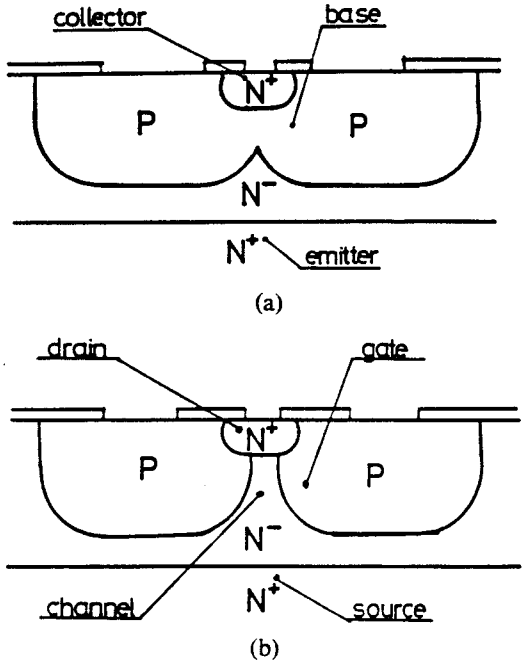

Fig. 1. The structures of new transistor types made by lateral p-diffusion.
(a) bipolar transistor.
(b) static induction transistor.

where

N_e, N_b—impurity concentration in emitter and base respectively

V_{be}—applied voltage to the base emitter junction

This potential barrier hight V_{h1} is independent on collector voltage (Early effect has secondary influence)

In the case of transistor structure presented in Fig. 1(b) the potential barrier for carrier injected from source is electrostaticaly induced by gate and drain potentials.

$$V_{h2}=\xi_1\left[\frac{kT}{q}\ln\left(\frac{N_sN_g}{n_i^2}\right)-V_g\right]+\xi_2\left[\frac{kT}{q}\ln\frac{N_s}{N_d}-V_d\right] \tag{4}$$

where

N_s, N_g, N_d—source, gate and drain impurity concentrations.

V_g, V_d—voltage applied to the gate and drain.

ξ_1, ξ_2—coefficients dependend on structure dimensions.
both ξ_1 and ξ_2 are lower than unity.

The high of this potential barrier V_{h2} (for the same voltage applied) is of course lower than V_{h1}. The structure presented in Fig. 1(b) can be operated then with lower supply voltages. This structure however will operate in logic circuits only when the drain potential influence on barrier hight is weaker than gate potential influence. (i.e. $\xi_1 > \xi_2$) This imposes the proper structure design. For negative and upto small positive gate potentials, the transistor presented in Fig. 1(b) operates as a Static Induction Transistor which was introduced by J. Nishizawa *et al.*[5] At still higher positive gate potentials, both holes from the gate and electrons from the source are injected into channel region. Because of the built-in field at the n^+n^- interface only the electrons can travel from the source of the drain, while the holes injected from the gate (for small drain voltages) create a static charge in the channel.

The following injection current for the structure presented in Fig. 1(b) can be marked out:

I_{hc}—hole injection current from gate to the channel region.

$$I_{hc}=\frac{n_i^2DA_cq}{N_cw}\exp\left(\frac{qV_g}{kT}\right) \tag{5}$$

I_{hs}—hole injection current from gate to the source.

$$I_{hs}=\frac{n_i^2DA_gq}{\int_0^{L_d}N_s\,dx+N_cd}\exp\left(\frac{qV_g}{kT}\right) \tag{6}$$

I_{eg}—electron injection current from source to the gate.

$$I_{eg}=\frac{n_i^2DA_gq}{\int_0^{x_j}N_g\,dx}\exp\left(\frac{qV_g}{kT}\right) \tag{7}$$

I_{ec}—electron injection current from source to the channel.

where

$$I_{ec}=I_{eg}\exp\left[\frac{q(V_{h2}-V_{h1})}{kT}\right] \tag{8}$$

w—channel width.

d—epitaxial layer thickness between gate and source.

x_j—depth of p-type diffusion.

V_{h1}, V_{h2}—are given by eqs. (3) and (4).

The currents I_{eg} and I_{hs} are very small, and also almost all injected holes from gate to the channel (eq. (5)) penetrate again to the gate region. Some of holes recombinate in channel region.

The gate current is then caused mainly by this hole-electron recombination in the channel region. Direct indection of carries both from the source to the gate (electrons) and from the gate to the source (holes) is comparatively small because of the presence of the built-in field. In a logic circuit this transistor operates in both of the modes-the SIT mode of the high output-voltage level and the gate injection mode for the low output-voltage level.

Both transistor structures from Fig. 1 applied for logic circuit will improve the switching performance. In case of transistor from Fig. 1 (a), the delay-power product can be lowered by one order of magnitude due to minimize both the base-emitter capacitance originated from lower doped epitaxial layer and the collector-base capacitance caused by specific impurity profile and especially large storage effect in the base region. Also the current gain for this *npn* transistor can be higher than in I^2L due to nonexistence of impurity gradient in the base.

The additional advantage of the transistor structure presented in Fig. 1(b) is that it can operate for smaller voltages which gives further decreasing in delay-power product.

§4. Three Mask Technology

As in usual cases the logic structure presented in Fig. 2(a) needs only four masking operations (*p*-diffusion, *n*-diffusion, contact holes, metalization). However because of this specific structure, wherein the entire wafer area can consist of either *p*-type diffused or *n*-type diffused region only, it is possible to use only one mask for both *p*-type and *n*-type diffusions. (Fig. 2(b)). One of the known technological methods can be used for this purpose, *e.g.* boron doped SiO_2, or Si_3N_4 masking. This reduction in the number of masking operations required permits further miniaturization of the devices. When the Si_3N_4 is used, the self-alignment process can be applied. Therefore, in the case of minimum size of the mask windows equal to 5 μm both the n^+ drain diffusion and contacts to the drains can have size of the order of 2 μm and alignment processes is not necessary. The simple structure make fabrication process easier and also small number of masking processes can lead to the good yield comparable with MOS technology.

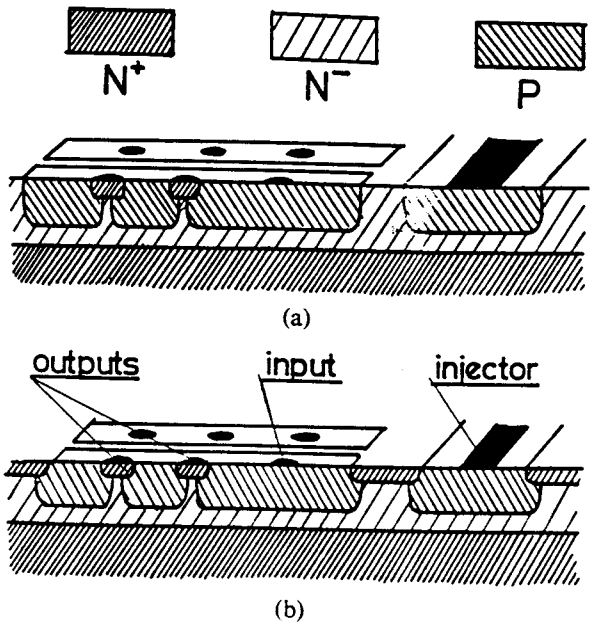

Fig. 2. The logic gate structures.
(a) using 4-mask technology.
(b) using 3-mask technology.

§5. High Packing Density

In the I^2L structure all gates must be isolated by a deeply diffused *n*-layer to prevent lateral injection between gates. This is especially because in I^2L structure the *npn* transistor current gain is low (inversed mode operation) which results in a very low noise margin and also small fan-out. Thus, if we do not use *n*-type isolation diffusion in the I^2L, the circuit may not operate at all. In the case of the proposed structure (Fig. 1(b)), the lateral injection between gates does not affect the circuit operation. On the contrary, this lateral injection between gates decreases the delay time, since the effective supply current is higher due to this effect. It

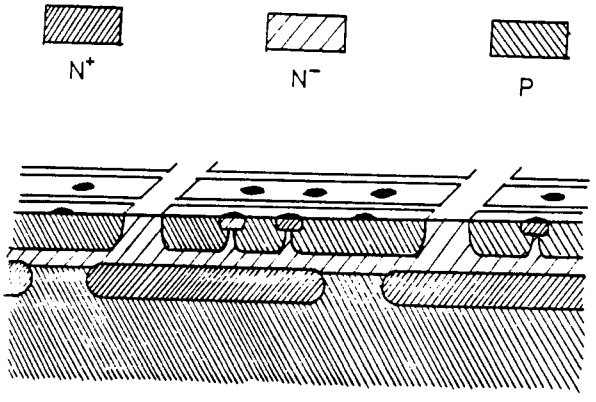

Fig. 3. Logic structure with high packing dencity using vertical injectors.

make that an *n*-type isolation diffusion layer is unnecessary. This permits very high packing densities upto 1000 double-output gates per mm^2. In the Fig. 3, a structure with vertical injectors similar to SFL[4] is shown. This modification allows for further increase in packing density, upto about 2000 gates per mm^2. Therefore the packing density is only limited by the metal interconection between gates.

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